DSD 2012
15th Euromicro Conference

Call for Papers

Special Session .....

Session Chairs:

Zdenek Kotasek
Brno University of Technology
Czech Republic

Special Session Program Subcommittee:

Ch. Bolchini, Politecnico di Milano (IT)
G. Di Natale, LIRMM (FR)
G. Fey, Univ. of Bremen (DE)
I. Koren, Univ. of Massachusetts (US)
Z. Kotasek, Brno U. of Technology (CZ)
H. Kubatova, CTU in Prague (CZ)
H. Manhaeve, Q-Star Test (BE)
I. Levin, Tel Aviv University (IL)
S. Racek, U. of West Bohemia (CZ)
J. Raik, Tallin U. of Technology (EE)
M. Rebaudengo, Pol. di Torino (IT)
G. Russell, U. of Newcastle u. Tyne (UK)
T. Sato, Fukuoka University (JP)
H. Shimada, Kyoto University (JP)
A. Steininger, Vienna U. of Techn. (AT)
H. T. Vierhaus, Brandenburg U. Tech. (DE)

Contact Information

Zdenek Kotasek,
Faculty of Information Technology,
Brno University of Technology,
Bozetechova 2,
612 66 Brno,
Czech Republic.
Tel.: +420 541 141 223
e-mail: kotasek@fit.vutbr.cz

Special Session on Fault Tolerance in Digital System Design

The Euromicro Conference on Digital System Design (DSD) addresses all aspects of (embedded) digital and mixed hardware/software system engineering. It is a discussion forum for researchers and engineers working on state-of-the-art investigations, developments and applications. It focuses on advanced system and design automation concepts, paradigms, methods and tools, as well as modern implementation technologies enabling an effective and efficient development of high-quality systems for demanding applications.
For demanding applications it becomes increasingly important to include fault tolerance features into the resulting design. For this purpose, various methodologies were developed for different design levels – the goal is to support dependability of components, units and systems.

Special Session Scope

Papers on any of the following and related topics can be submitted to the special session:

- Defect/fault tolerant architectures (SoCs, NoCs, embedded systems).
- TMR based designs.
- Dependability modeling, dependability analysis and validation.
- Design for testability in fault tolerant systems.
- FPGA based fault tolerant systems, partial/full reconfiguration based methodologies.
- Single-event upsets and effects, single-event transients.
- Fault injection techniques. Reliability analysis.
- On-line testing, design of checkers.
- Communication protocols testing.
- Reliable IP cores.
- Fault tolerance in nanotechnologies.
- Fault tolerant design in practical applications. Reliable applications.
- Functional safety and IEC 61508.

Submission Guidelines

Prospective authors are encouraged to submit their manuscripts for review electronically through the following web page (http://www.easychair.org/conferences/?conf=dsd2012) or by sending the paper to the Session Chair via email (kotasek@fit.vutbr.cz) only if an unexpected web access problem is encountered before the deadline for submission.
Each manuscript should include the complete paper text, all illustrations, and references. The manuscript should conform to the required IEEE format: single-spaced, double column, A4/US letter page size, 10-point size Times Roman font, up to 8 pages. In order to conduct a blind review, no indication of the authors' names should appear in the submitted manuscript, references included.

The IEEE Conference Publishing Services (CPS), Conference Publishing Services, publishes the DSD Proceedings, which are available worldwide through the IEEE Xplore Digital Library. An extended version of the best papers will be published in a special issue of the ISI-indexed *"Microprocessors and Microsystems: Embedded Hardware Design"* journal, printed by Elsevier

Important Dates

- **Submission of papers: March 26th, 2012**
- Notification of acceptance: May 7th, 2012
- Camera ready papers: May 31st, 2012

Web Links

- DSD'12 web page:
- ***www.univ-valenciennes.fr/dsd2012/***
- Euromicro web page:
  http://www.euromicro.org