

SESSION CHAIRS:

J. Sahuquillo, Univ. Politécnic de Valencia, Spain
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SPECIAL SESSION PROGRAM

SUBCOMMITTEE:

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SPECIAL SESSION ON MULTICORE SYSTEMS: DESIGN AND APPLICATIONS (MSDA)

The microprocessor industry moved to multicore systems, as an efficient alternative to reduce power consumption while improving the performance. These systems are dominating a wide spectrum of the microprocessor market, ranging from high-performance computers to embedded systems. Several commercial products already implement more than ten cores in a single chip, and this number is expected to rise in future microprocessor generations.

Although these systems can potentially provide significant performance benefits, in practice, exploiting the multicore's inherent resources represents an important challenge for researchers and engineers. In this context, load balancing and scheduling policies are required to take advantage of the whole system. Memory hierarchy concepts must be revisited to improve, among others, the efficiency of the last level cache, the efficiency of replacement/placement algorithms, and NUCA cache performance. Interconnect must be simpler and faster than ever in order to reduce the latencies. Compilers must improve the efficiency of both sequential code and parallel code, taking into account proximity among cores.

SPECIAL SESSION SCOPE

This special session will provide a forum for engineers and scientist to address challenges, and present new ideas in the multicore field, as well as introduce emerging implementations, and tackle related issues with respect to improving system performance and reducing energy consumption for multicore systems, as a whole.

Authors are invited to submit high quality papers representing original work in (but not limited to) the following topics targeting multicore multithreaded processors:

- Multicore and multithreaded architectures: concepts, design, (FPGA) implementation, case studies.
- Scheduling and workload balancing.
- Multicore programming.
- Power-aware architectures and computing.
- Thermal and temperature aware architectures.
- Embedded multicore real-time systems.
- Memory hierarchy: last level cache management, placement/replacement algorithms, NUCA, and main memory.
- Coherence protocols, scalability and power consumption.

SUBMISSION GUIDELINES

Prospective authors are encouraged to submit their manuscripts for review electronically through the following web page (<http://www.easychair.org/conferences/?conf=dsd2012>) or by sending the paper to the Session Chair via email (jsahuqui@disca.upv.es) only if an unexpected web access problem is encountered) before the deadline for submission.

Each manuscript should include the complete paper text, all illustrations, and references. The manuscript should conform to the required IEEE format: single-spaced, double column, A4/US letter page size, 10-point size Times Roman font, up to 8 pages. In order to conduct a blind review, no indication of the authors' names should appear in the submitted manuscript, references included.

The IEEE Conference Publishing Services (CPS), Conference Publishing Services, publishes the DSD Proceedings, which are available worldwide through the IEEE Xplore Digital Library. An extended version of the best papers will be published in a special issue of the ISI-indexed "Microprocessors and Microsystems: Embedded Hardware Design" journal, printed by Elsevier Ltd.

IMPORTANT DATES

- **Submission of papers: March 26th, 2012**
- Notification of acceptance: May 7th, 2012
- Camera ready papers: May 31st, 2012

WEB LINKS

- DSD'12 web page:
www.univ-valenciennes.fr/dsd2012/
- Euromicro web page:
<http://www.euromicro.org>