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SPECIAL SESSION PROGRAM

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SS5: SPECIAL SESSION ON

SYSTEM-LEVEL ENERGY OPTIMIZATION OF EMBEDDED SYSTEMS (SLEO)

Power consumption is becoming the main factor limiting the processing capability of embedded systems. Currently, most of the embedded systems are based on multi-processing platforms such as Systems-on-Chip (SoCs), board-based systems (PCBs) or Wireless Sensor Networks (WSNs). SoC and PCB based systems often execute complex application SW in close interaction with the HW resources of the complete platform. Power estimation and optimization in these heterogeneous platforms is a research area of increasing importance. Many optimization strategies have been proposed in the past, especially at the algorithmic level. More research activity is needed in order to be able to address the increasing complexity and heterogeneity of current and future massively concurrent, many-cores, HW/SW Embedded Systems. Another application domain where power optimization is very important is Wireless Sensor Networks (WSN). WSNs offer the promise of cost-effective solutions for sensing and communicating data in many application domains, and a growing number of industrial players are providing integrated solutions that mix advanced sensor technologies with ad-hoc communication capabilities. Information and data processing issues, resource-efficient implementation infrastructures, programming models, power-aware system-level design, and design automation play an increasingly important role in the WSN field and deserve careful attention.

SPECIAL SESSION SCOPE

This special session aims at gathering within the same forum contributions regarding the optimization of the energy at the system-level, novel techniques for energy optimization and power reduction of embedded systems and wireless sensor networks are sought. Papers on any of the following and related topics will be considered for the special session:

Mechanisms and Policies for resource management at system level, Power-aware system-level HW/SW co-design, Power modeling and estimation, Task-level optimization of software power consumption, Performance-energy-cost tradeoffs, Architectural solutions to reduce power consumption on multiprocessing platforms, Power aware computation, Load balancing in multiprocessor architectures, Power aware communication in SoC with NoC, Energy aspects in multimedia, communications, networking and other current applications, Wireless sensor networks, Body-area networking, Low-power applications in transport and mobility, Agriculture, Environmental and urban monitoring, Healthcare and elderly care, Home automation and assisted living, Design/use of energy aware software libraries and standards.

SUBMISSION GUIDELINES

Prospective authors are encouraged to submit their manuscripts for review electronically through the following web page (<http://www.easychair.org/conferences/?conf=dsd2012>) or by sending the paper to the Session Chair via email, only if an unexpected web access problem is encountered) before the deadline for submission (villar@teisa.unican.es).

Each manuscript should include the complete paper text, all illustrations, and references. The manuscript should conform to the required IEEE format: single-spaced, double column, A4/US letter page size, 10-point size Times Roman font, up to 8 pages. In order to conduct a blind review, no indication of the authors' names should appear in the submitted manuscript, references included.

The IEEE Conference Publishing Services (CPS), Conference Publishing Services, publishes the DSD Proceedings, which are available worldwide through the IEEE Xplore Digital Library. An extended version of the best papers will be published in a special issue of the ISI-indexed "Microprocessors and Microsystems".

IMPORTANT DATES

- **Submission of papers: March 26th, 2012**
- Notification of acceptance: May 7th, 2012
- Camera ready papers: May 31st, 2012

WEB LINKS

- DSD'12 web page:
- www.univ-valenciennes.fr/dsd2012/
- Euromicro web page:
<http://www.euromicro.org>