FPGA Hardware in the Loop System for ERTMS-ETCS Train Equipment Verification

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Outline

• Introduction
  – ERTMS standard
  – Actual equipment
  – Requirements and standardization

• Motivation and cause
  – Testing of equipment
  – Limitations

• Proposed solution
  – Hybrid architecture
  – Network of cards
  – Interface to train equipment
  – Testing scenarios

• Results
Introduction

• European Rail Traffic Management System (ERTMS)
  - Standard to unify European train and traffic signalizations.
  - Decomposition:
    • European Train Control System (ETCS).
    • GSM-R mobile communication unit.
Introduction

- The decomposition of the ERTMS equipment
  - ETCS
  - GSM-R
Introduction

- Requirements and standardization
  - This work concerns the **EVC testing**
  - Real time data mimicking real scenarios
  - Real communication ports (RS422, COAX...) mimicking real sensors
  - Real interface display (DMI)

**Conclusion**: propose a system that mimics the rail and the driver environment
Motivation

• Existing testing system:
  – Test scenario simulator (MultiRailLab) running on a Windows 7, Intel Core i7 2.4 GHz with 8 GB RAM.
  – Simulator draws speed profile, balise locations, telegram contents and radio transceivers locations.
  – Simulator surveys EVC speed readings, decode emitted balises telegrams at specified locations and verify radio transactions (information).

• Limitations:
  – Special ports communication with EVC (RS485, RS232, COAX…)
  – Real time constraints. Example: 24 Bytes (information and CRC) frames each 20 msec
Proposed Solution

- An intermediate system that can ensure real time constrains and real port configuration
Proposed Solution

- Hybrid architecture proposition:
  - Ethernet is easier when using a **processor** card
  - FPGA are great candidates for real time **constraints**, are **configurable** and **adaptable**
  - This configuration allows **remote** debugging and configuring

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<table>
<thead>
<tr>
<th>SBC Tegra 2</th>
<th>FPGA Cyclone II</th>
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Common board
Proposed Solution

- ERTMS
- Equip.
- Requir.
- Motivation
- Testing
- Real time
- Proposed solution
- Hybrid archi.
- Network of cards
- Interface to equip.
- Testing scenarios

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Proposed Solution

- Testing scenarios:
  - Real time constraints by verifying CDS time tags compared to the simulator configuration
  - Test communication ports transmissions and reception correct functionality
  - Verify ODO speed signals to DMI and telegrams
  - BSG transmitter signals
Results

• Acquired results, advantages and solutions
  – Easy to use software to EVC testing while the complicated intermediate hardware system is invisible
  – Remote updates and testing possibilities
  – Easy to adapt to new communication ports/standard by replacing the application board and updating the software of the common board
  – Reliable test environment before deployment
    • Real-time simulations
    • Real EVC communication ports
  – Cost reduction with new reduced time-to-market thanks to new FPGA development tools
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Thank You